X4 - Errata

Rev. B - 12-Feb-2023

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1. IC Anomalies Overview

This section lists the anomalies found in the different revisions of the X4 IC.

ID	Module	Description	Affects X4 revision
001	Timing	PLL may in rare cases fail to lock.	1,2
002	Power	Power-down current may increase to several hundred µA.	1,2,3

Table 1.1. IC Anomalies Overview

2. [001] - PLL may in rare cases fail to start

This anomaly applies to IC revisions 1 and 2.

This anomaly is fixed in IC revision 3.

The X4F103 module is manufactured only with X4 IC revision 3. The anomaly does as such not affect X4F103. The symptoms and workarounds described below are only relevant for older Novelda sensor modules and older Novelda SW (XEP SW).

2.1. Description

The VCO in the RX and TX PLLs on the device may in very rare cases fail to start oscillating when the PLL is powered on. The problem is caused by the ring VCO entering a non-oscillating steady state. Once the VCO has entered the non-oscillating state, the entire PLL needs to be powered down before it can be re-started, as it is unable to exit the failed state on its own.

Leaving the PLL in the non-oscillating state may accelerate the degradation of the gates in the VCO, due to high current density in the ring oscillator. Remaining in this state for an extended amount of time may cause permanent damage.

2.2. Symptoms

The PLL lock signal is never asserted after starting the PLL. This is manifested in SW by the functions x4driver_setup_default() and x4driver_init() returning XEP_ERROR_X4DRIVER_COMMON_PLL_LOCK.

2.3. Conditions

The likelihood of entering the non-oscillating state increases with higher supply voltage.

A device in the non-oscillating state may be damaged quicker at higher supply voltages.

2.4. Workaround

Do not power on the RX and TX PLLs by writing directly to the PLL control register over SPI. Instead, use the new PLL startup procedure implemented in version 11 of the X4 firmware. The new version of the x4driver software, provided by Novelda, includes the updated X4 firmware, and is using the recommended PLL startup procedure.

The recommended PLL startup procedure detects if the PLL does not lock within the expected time and then powers down the PLL, waits for a predefined amount of time to allow oscillations and voltages to drop, and then attempt to start the PLL again. Multiple startup attempts are done with a varying delay between power-down and startup.

In addition to the firmware workaround, the supply voltage should be limited to 1.8 V.

3. [002] - Power-down current may increase to several hundred µA

This anomaly applies to IC revisions 1, 2 and 3.

3.1. Description

The power-down current (the current consumption when the Enable pin is pulled low) may in rare cases increase beyond the typical datasheet value to several hundred µA.

The anomaly is caused by two different mechanisms in the device:

1. IO5 and IO6 LVDS buffer leakage

2. Leakage in an analog test mux

The first mechanism is resolved by connecting IO5 and IO6 to ground.

The second mechanism only appears in Power-down, when the Enable pin is pulled low. It does not affect current consumption in any other power states.

The anomaly does not have any impact on device lifetime.

3.2. Symptoms

The power-down current increases.

3.3. Conditions

The issue can happen under all conditions.

3.4. Workaround

• Connect IO5 and IO6 to ground.

• If Power-down is required as a low power state it is recommended to remove voltage from the power supply pins during Power-down.

  Refer to the product specific SW documentation for information on which power modes is used in which states.

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Document History

Rev.	Release date	Change description
B	12-Feb-2023	Adding anomaly 002
A	01-July-2021	First release